

A Fully Integrated 24-GHz 8-Path Phased-Array Receiver in Silicon

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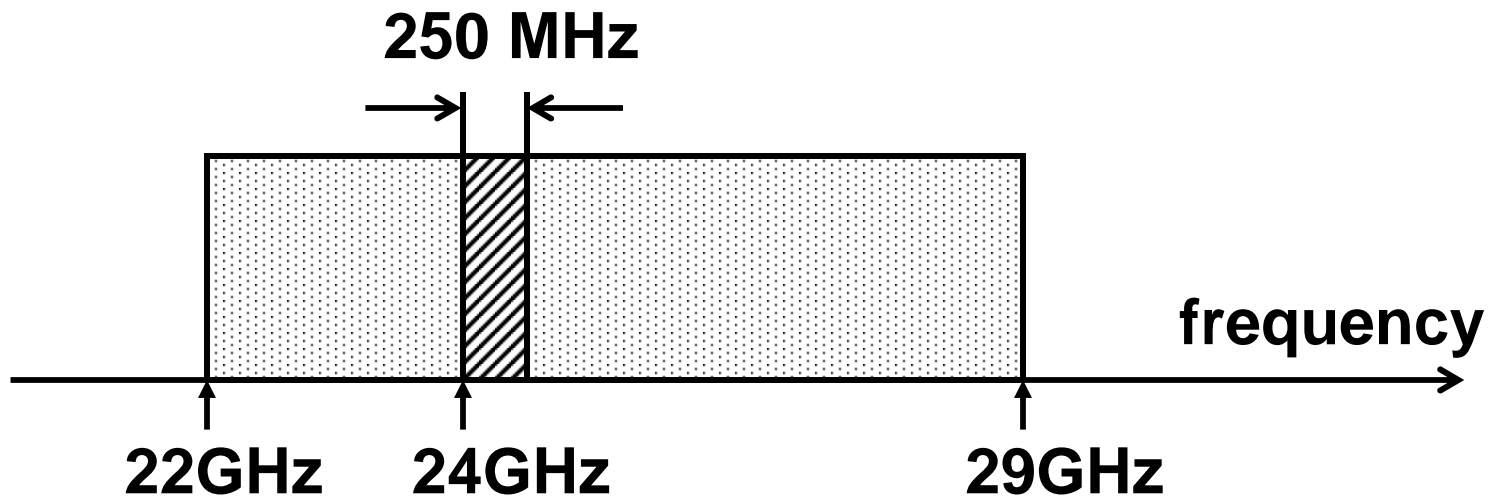
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
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Outline

- **Introduction**
- Phased-Array Receiver Architectures
- A 24GHz Integrated Phased-Array Receiver
- Measurement Results
- Conclusion

The 24-GHz Frequency Band



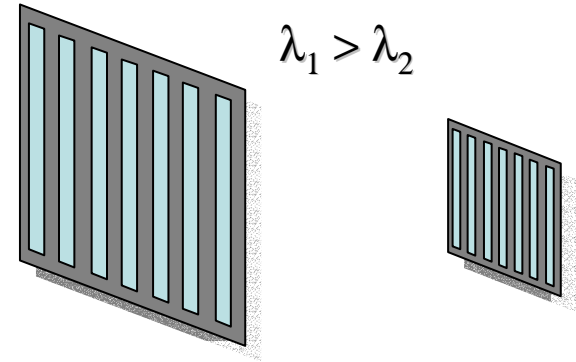
-  Industrial, Scientific, Medical (ISM) / Unlicensed*
-  Ultra Wide Band (UWB) for Vehicular Radar Systems

* 24.075 - 24.175GHz for field disturbance sensors (FCC Part 15, Section 15.245)
24.0 - 24.25GHz for fixed and point-to-point operation (FCC Part 15, Section 15.249)

24-GHz Compared to 2.4- and 5.2-GHz

- Smaller wavelength

- Reduced antenna size and spacing ($\sim \lambda$)
- Lower effective antenna area ($\sim \lambda^2$)



- Indoor channel characteristic in an office environment ¹:

- More isolation between floors
- Less delay spread for line-of-sight
- Comparable excess path loss for line-of-sight

- Less than proportionate increase of power consumption in a narrowband integrated radio implementation

¹ D. Lu and D. Rutledge, "Investigation of Indoor Channels from 2.4GHz to 24GHz," *IEEE International Antennas and Propagation Society Symposium, June 2003.*

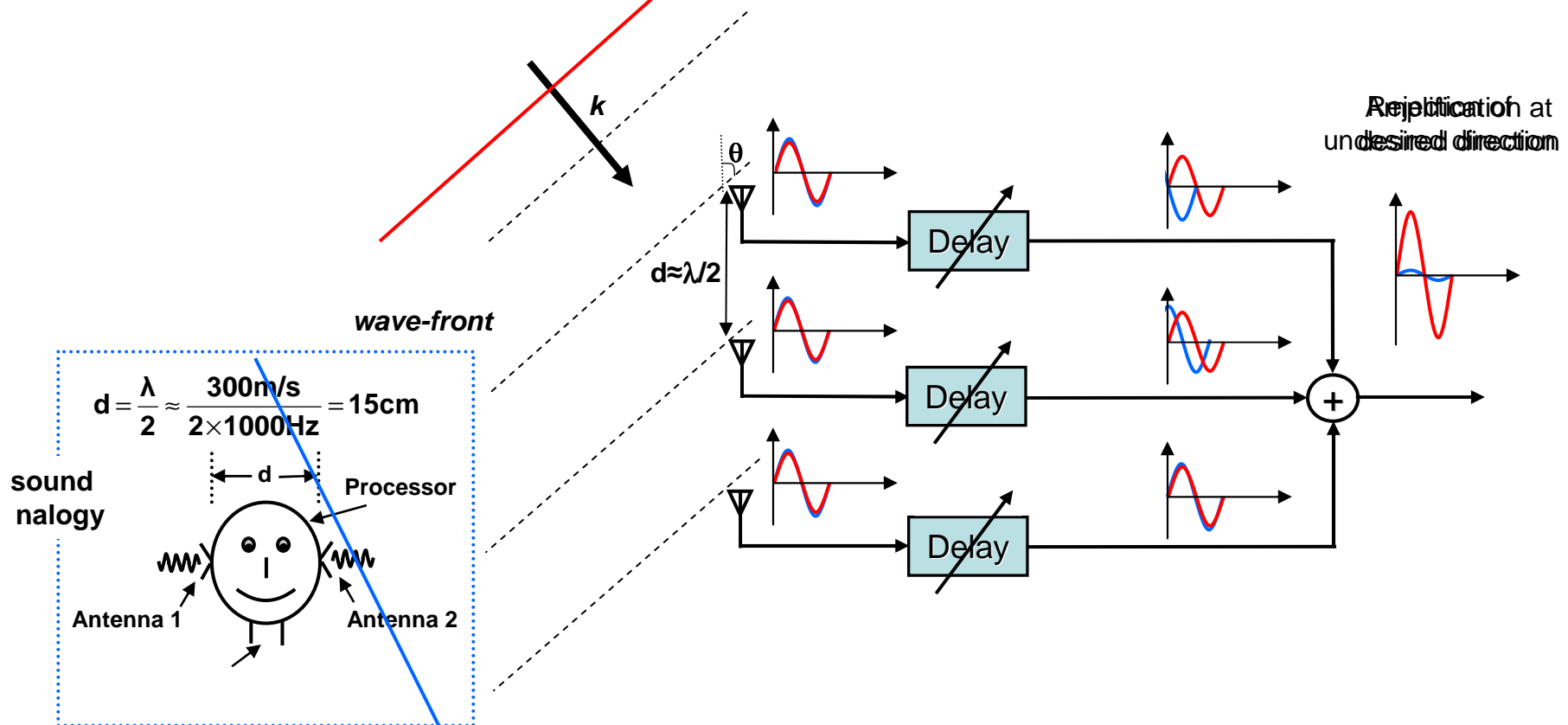
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Advantages of Multiple Antennas

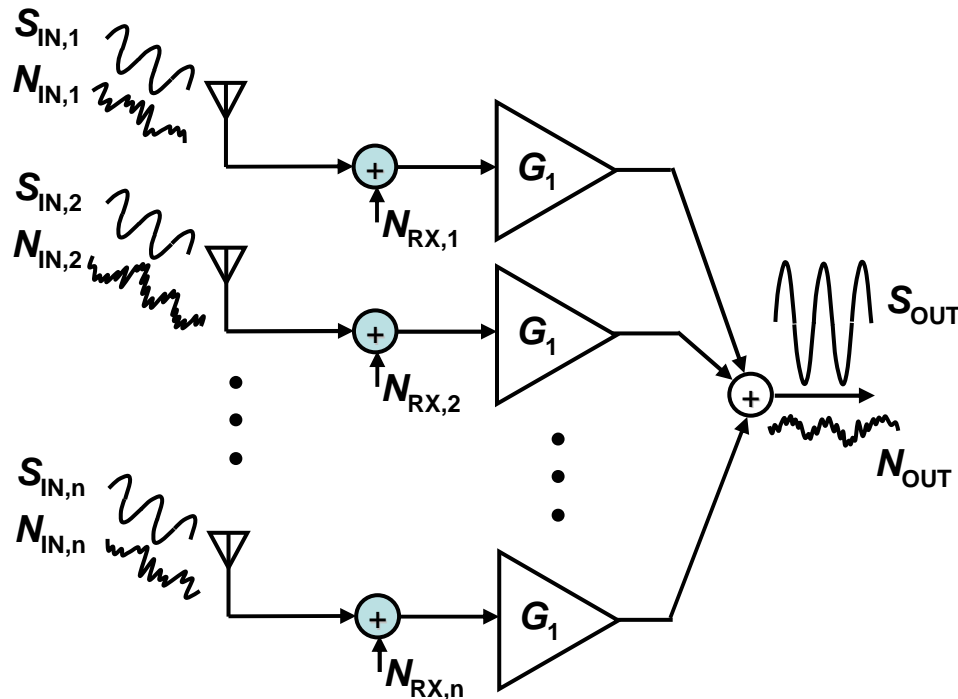
- Limiting factors in high speed wireless communications:
 - Multi-path Fading
 - Co-channel Interference
- Multiple spaced antennas form statistically independent communications channels in a fading environment.
 - Receiver diversity
 - Transmitter diversity
- Phased array provides a directional communication channel.
- Improvement increases with the number of antenna elements.

Phased-Array Principle



- Compensate for air propagation delay in order to amplify or reject signals from certain directions.
- Amplitude control allows for multiple spatial peaks and nulls.

Signal-to-Noise Ratio Improvement



$$S_{OUT} = G \cdot n^2 \cdot S_{IN}$$

$$N_{OUT} = G \cdot n \cdot (N_{IN} + N_{RX})$$

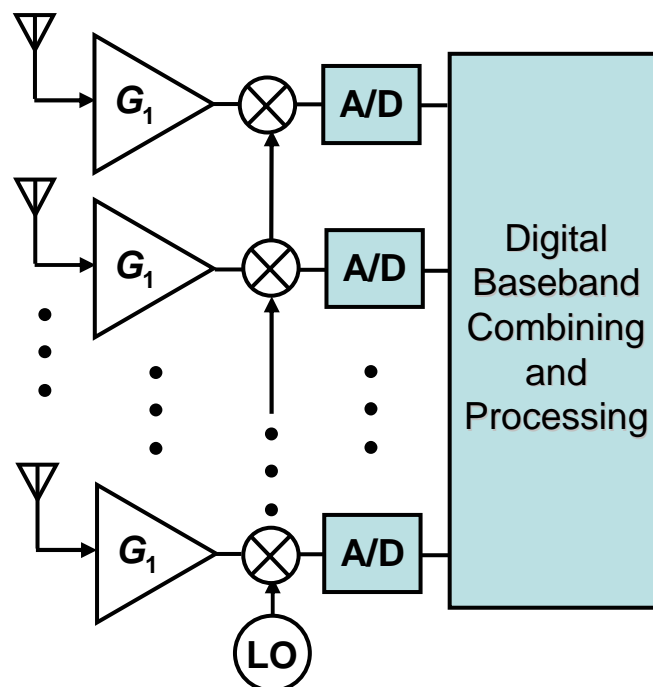
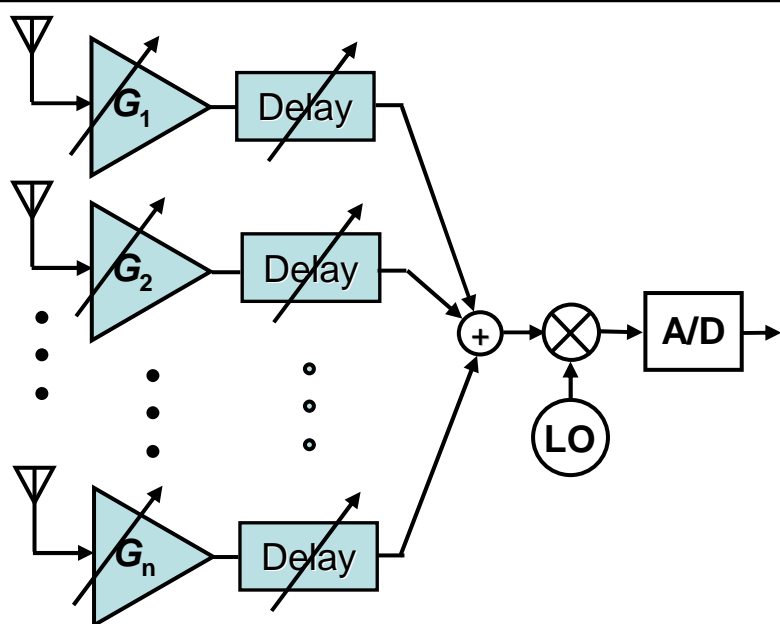
$$SNR_{OUT} = n \frac{S_{IN}}{N_{IN} + N_{RX}}$$

Example: $n=8$, $SNR_{IN}=6\text{dB}$, $BW=250\text{MHz}$, $NF_{1\text{-path}}=10\text{dB}$

$$\begin{aligned} \text{sensitivity} &= 10\log[C/(I+N)] + 10\log(k_B TB) + NF \\ &= (6 + \mathbf{9}) + (-174 + 84) + 10 \quad [\text{dBm}] \\ &= -65 \text{ dBm} \end{aligned}$$

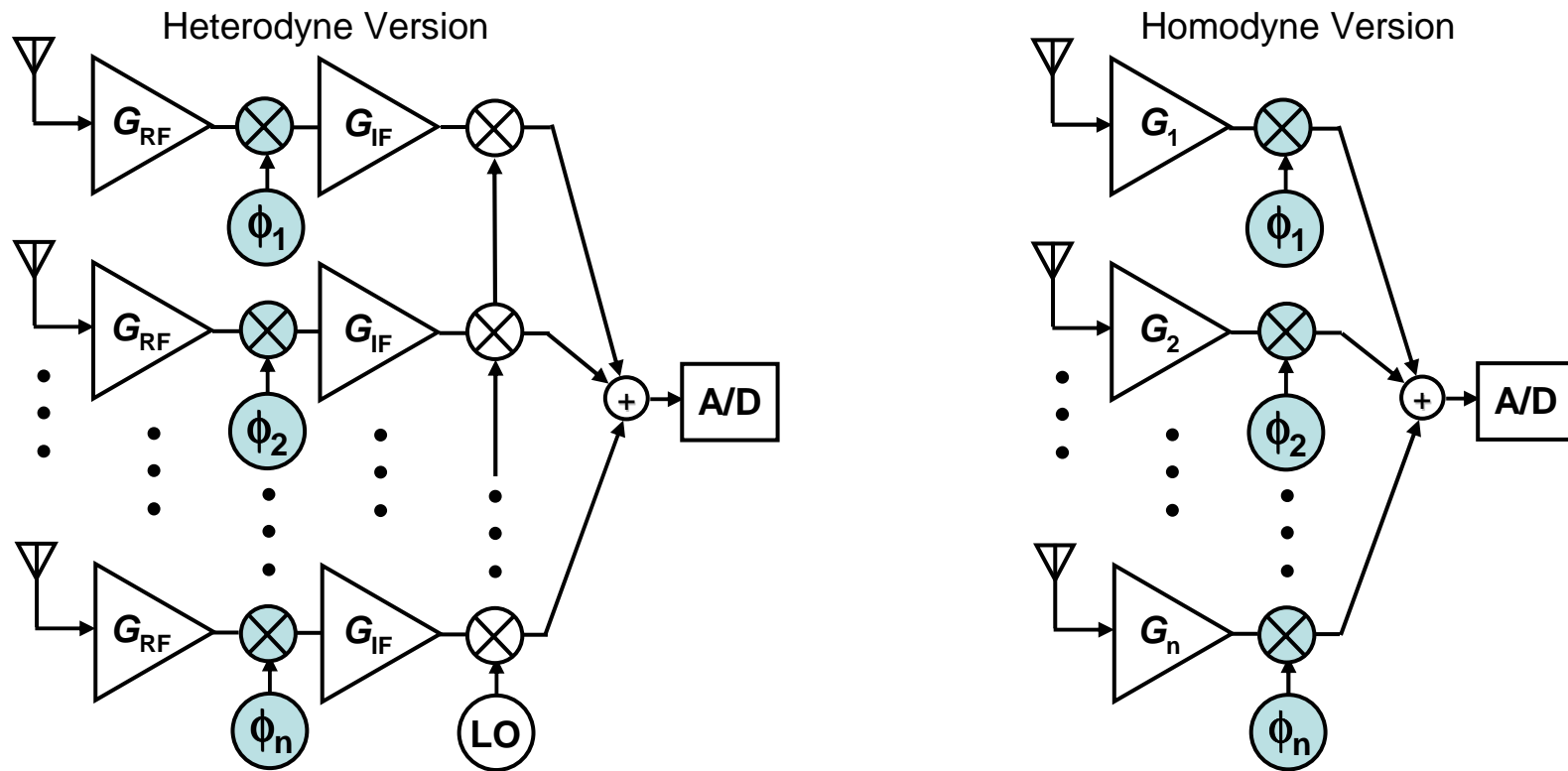
* Assuming equal input signal and noise power levels and identical paths.

Signal Path Phase Shifting Architectures



	<i>RF Phase Shifting</i>	<i>Baseband Processing</i>
Linear RF Phase Shifters	High	None
A/D Requirements	Low / Moderate	Severe
Power Consumption	Moderate	High
Analog Dynamic Range	High	Low
Versatility	Low	High

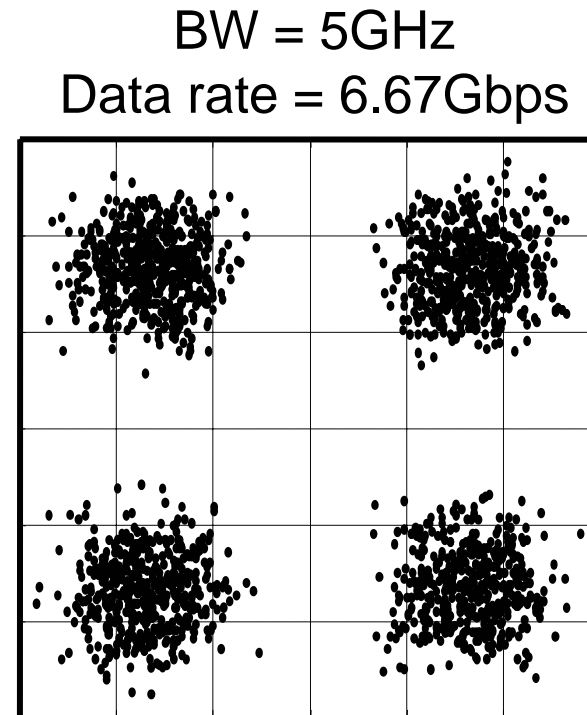
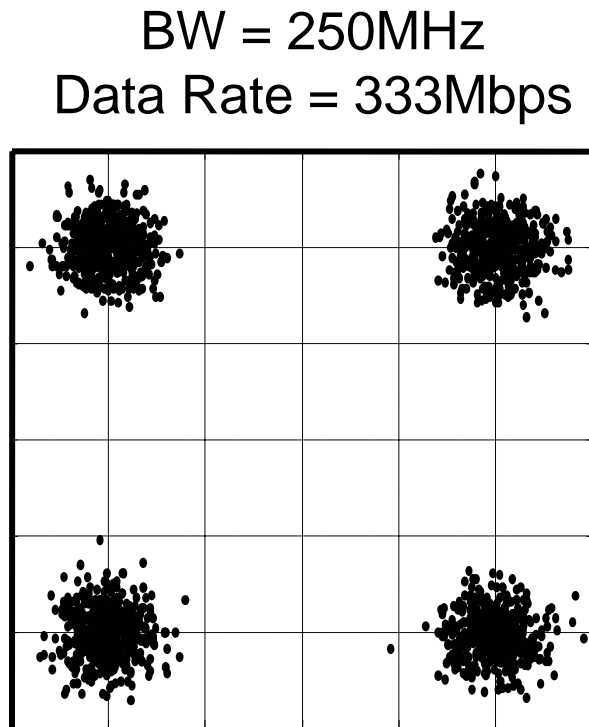
LO Phase Shifting Architecture



- Compensate propagation delay by phase shifting the LO,
- Ideal for narrowband channels,
- Accuracy is inversely proportional to the bandwidth.

Narrowband vs. Wideband

Signal constellations of a QPSK signal with 6dB SNR at each antenna input of an 8-path array at 24-GHz carrier frequency.*



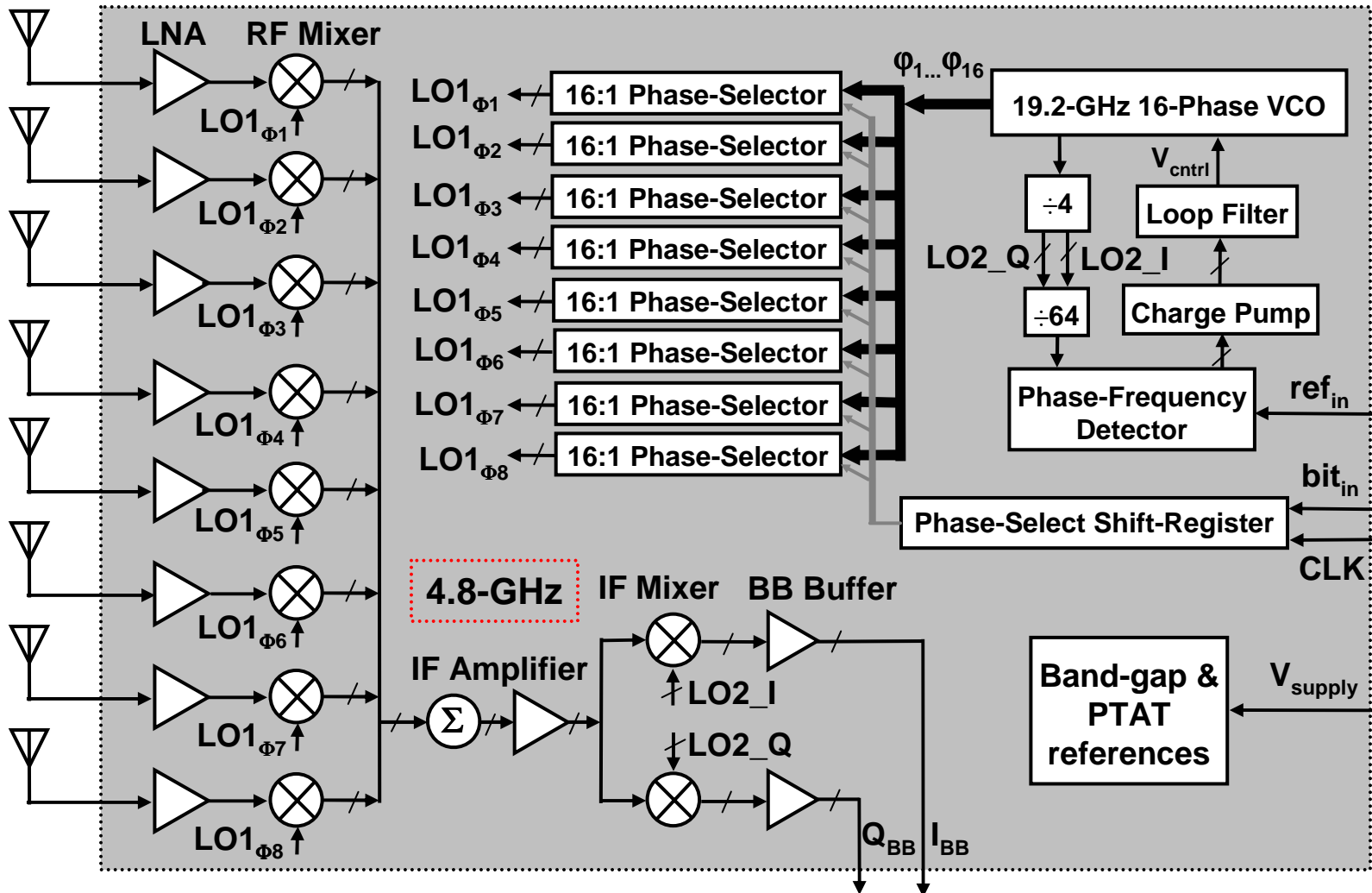
* Courtesy of Abbas Komijani, Caltech.

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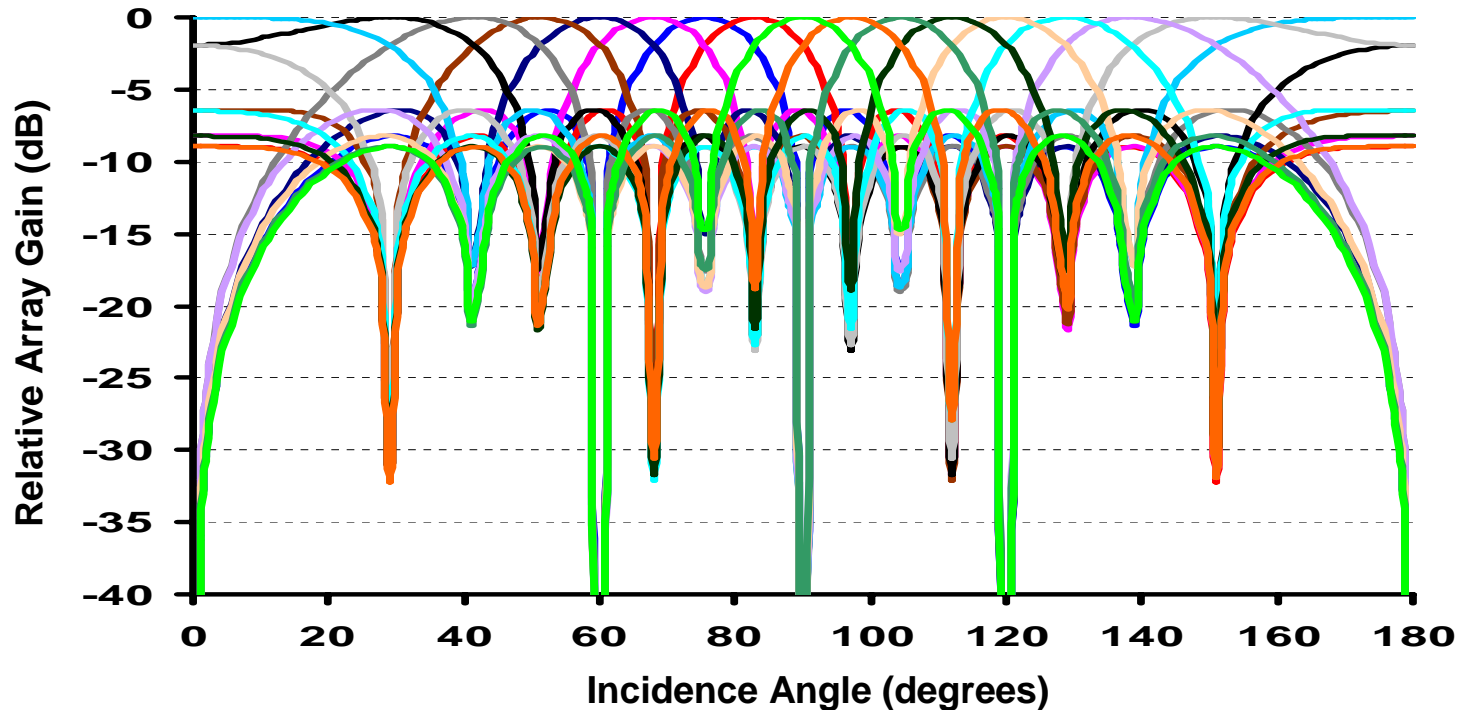
24GHz 8-Path Phased-Array Receiver

24-GHz



75-MHz

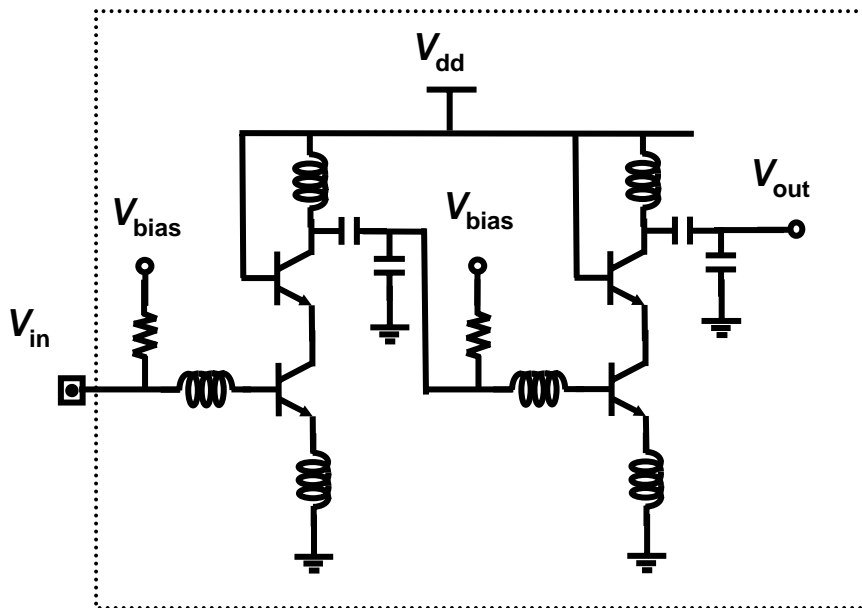
Beam Steering w/ Discrete LO Steps



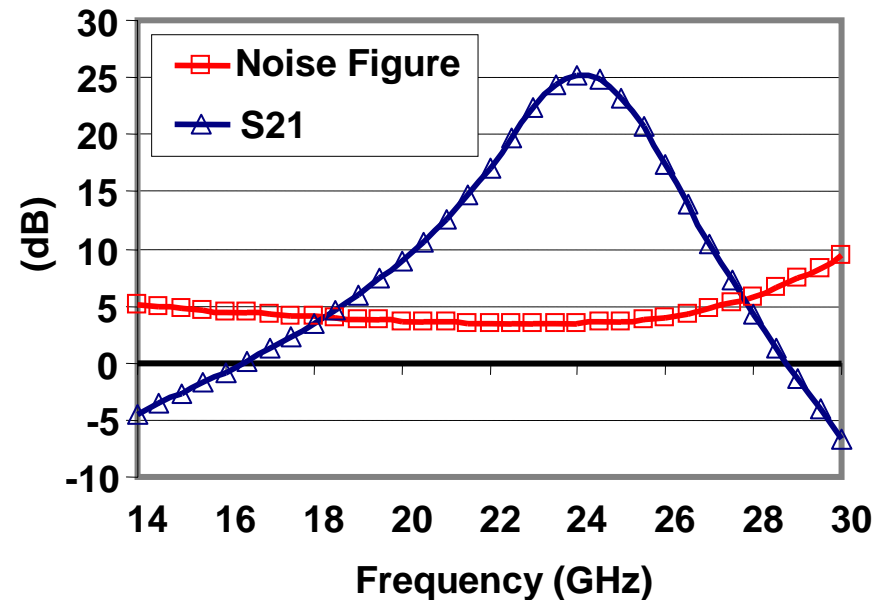
- 4-bit phase selection resolution,
- Forward looking beam steering steps of $\sim 10^\circ$,
- Sufficient coverage of the entire range of angles,
- Narrow beam width provides spatial selectivity,
- Nulls affected by asymmetric LO phase distribution.

24-GHz Two-Stage Low Noise Amplifier

One Signal Path

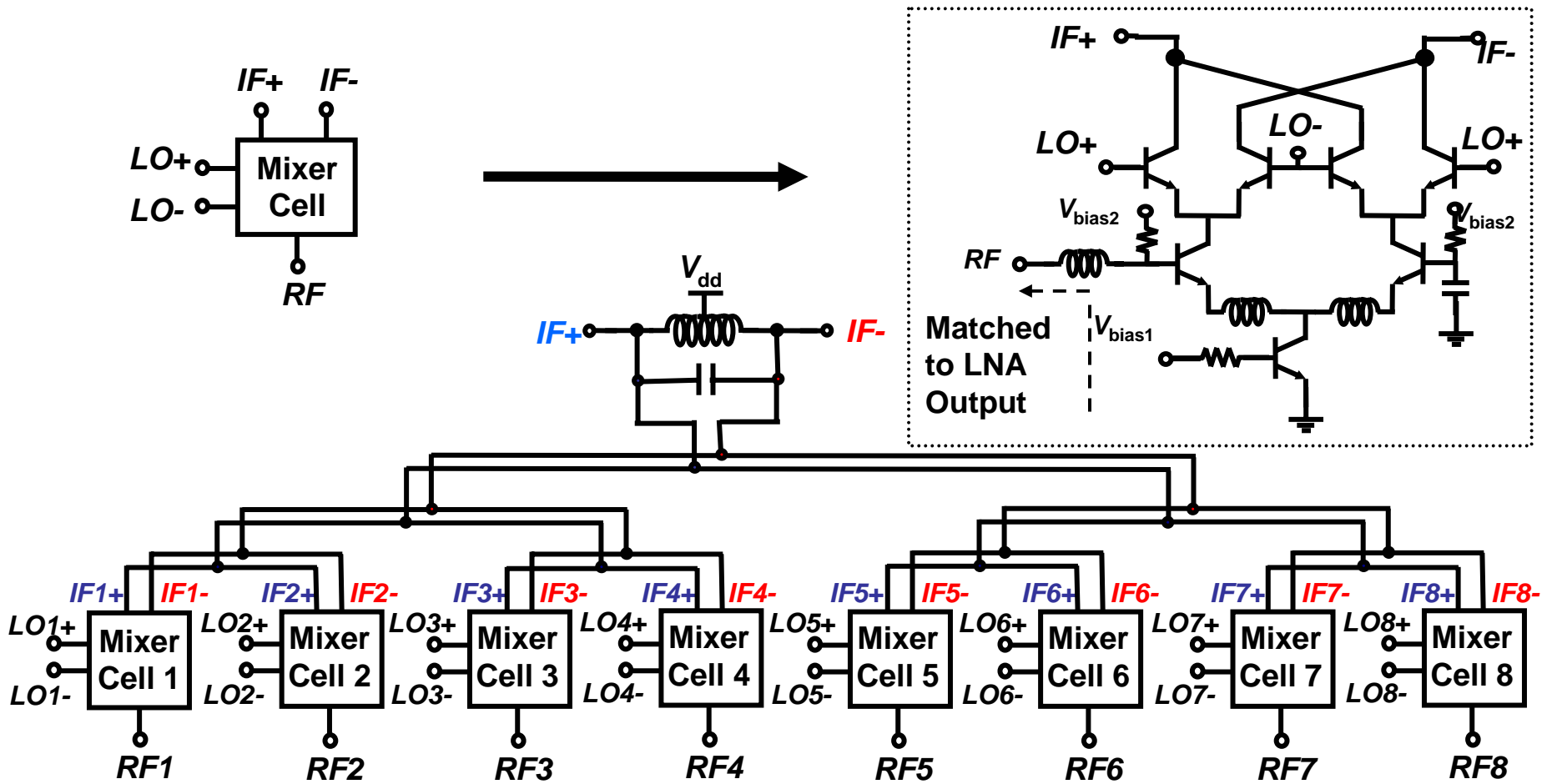


Simulated Performance



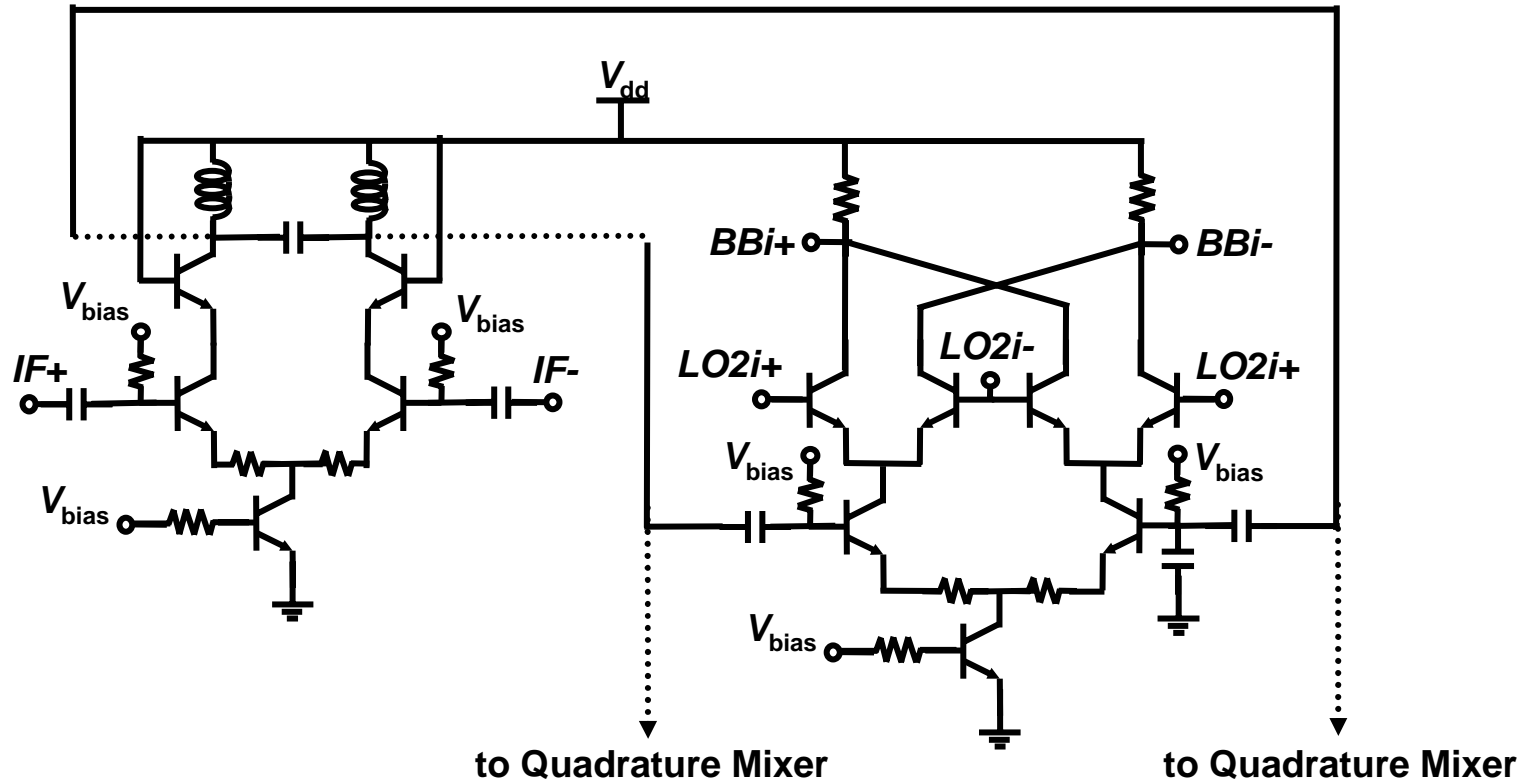
- Simultaneous noise and power match for the LNA,
- Impedance match between stages for max power transfer,
- 8-mA DC current consumption from a 2.5-V supply.

RF Mixers and IF Combining Structure



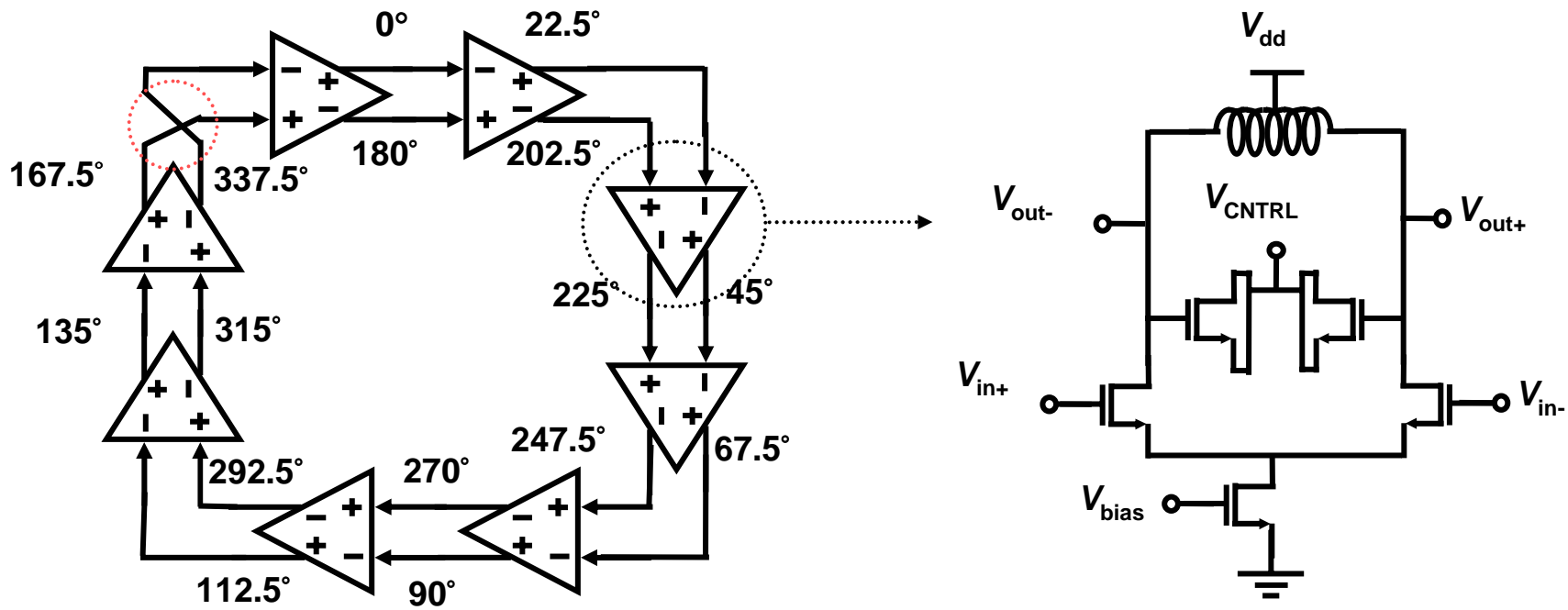
- Mixer outputs combined in current domain via a binary tree.

IF Amplifier and Image-Reject Mixers



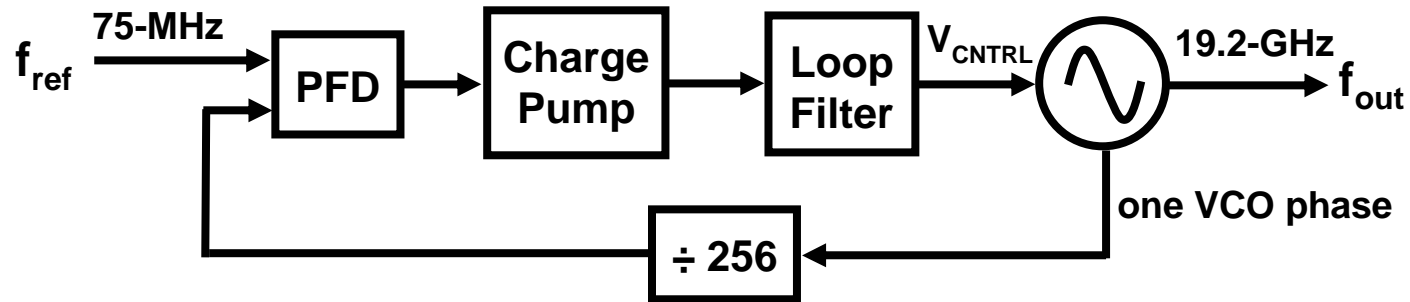
- The intermediate frequency is 4.8-GHz,
- Tuned loads at IF.

16-Phase Voltage-Controlled Oscillator



- 16-phase, 19.2-GHz CMOS VCO,
- An 8-stage ring structure generates 16 equally spaced phases,
- Single pole gain stage would require GBW larger than 46-GHz,
- Amplifiers tuned close to ω_{osc} due to large tank Q,
- Symmetric layout minimizes relative deviation of phases.

19-GHz Integer- N Frequency Synthesizer

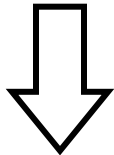
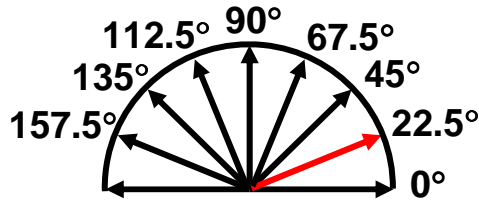


- Third order loop,
- Bandwidth of 7-MHz and settling time less than 50 μ s,
- Multi-switch charge pump to minimize reference feedthrough,¹
- Standard tri-state frequency phase detector (PFD),
- Master-slave latches with emitter controlled logic (ECL) for divide-by-two circuits.

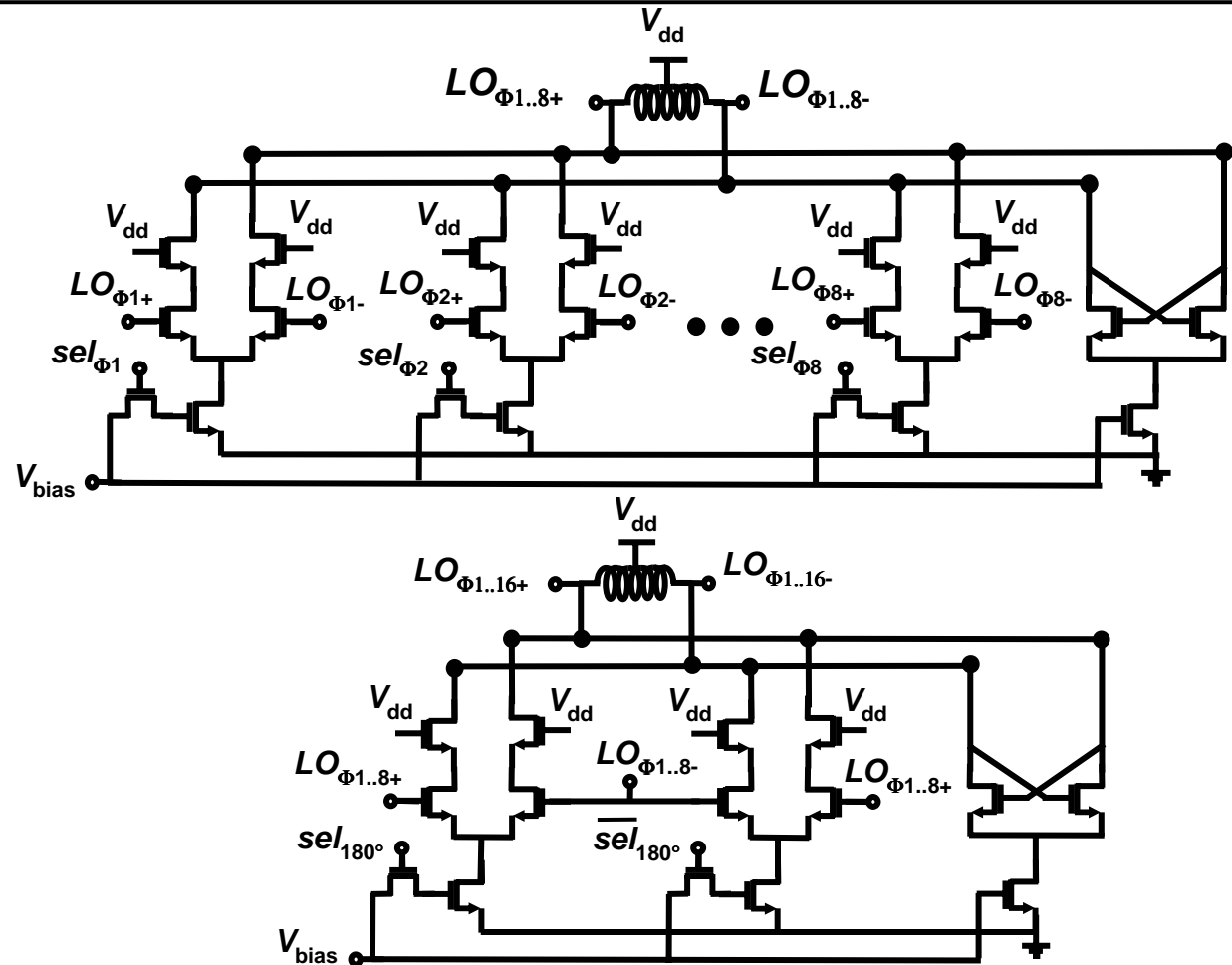
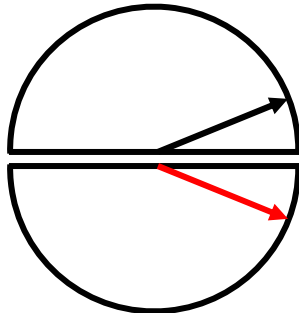
¹ J. Cranincks and M. Steyaert, "Wireless CMOS Frequency Synthesizer Design," *Kluwer Academic Publishers*, 1998.

Phase-Selecting (analog multiplexing)

Phase-Selector



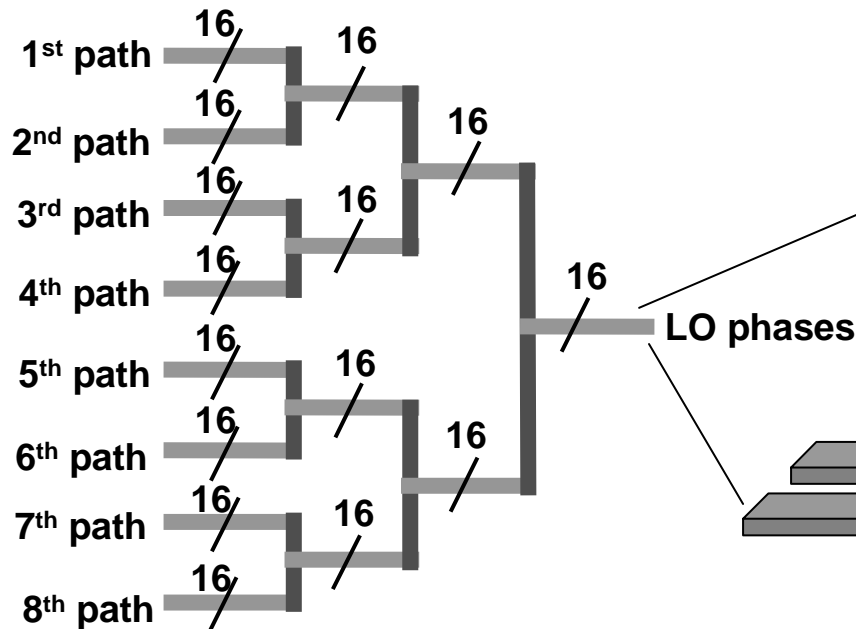
Sign-Selector



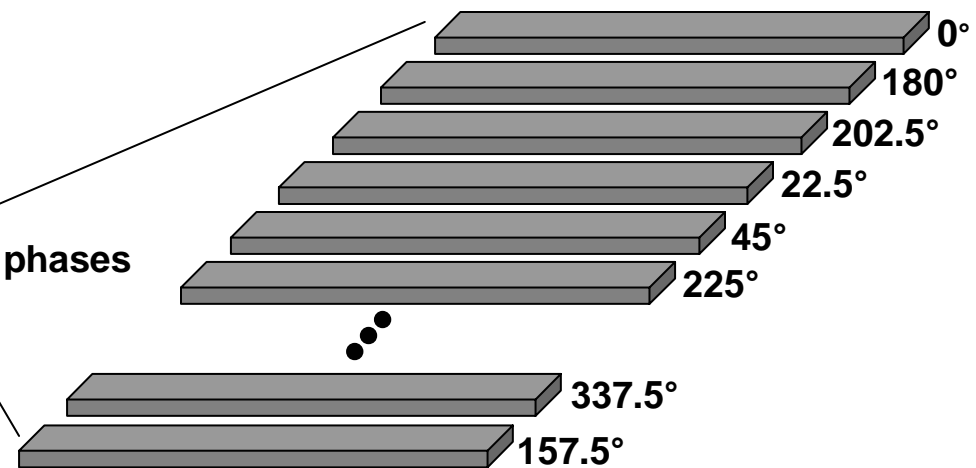
- $2^3+2=10$ total phase selectors instead of $2^4=16$,
- A dummy array is included to maintain constant loading

Oscillator Phase Distribution Network

Global Distribution Tree



Transmission Line Array



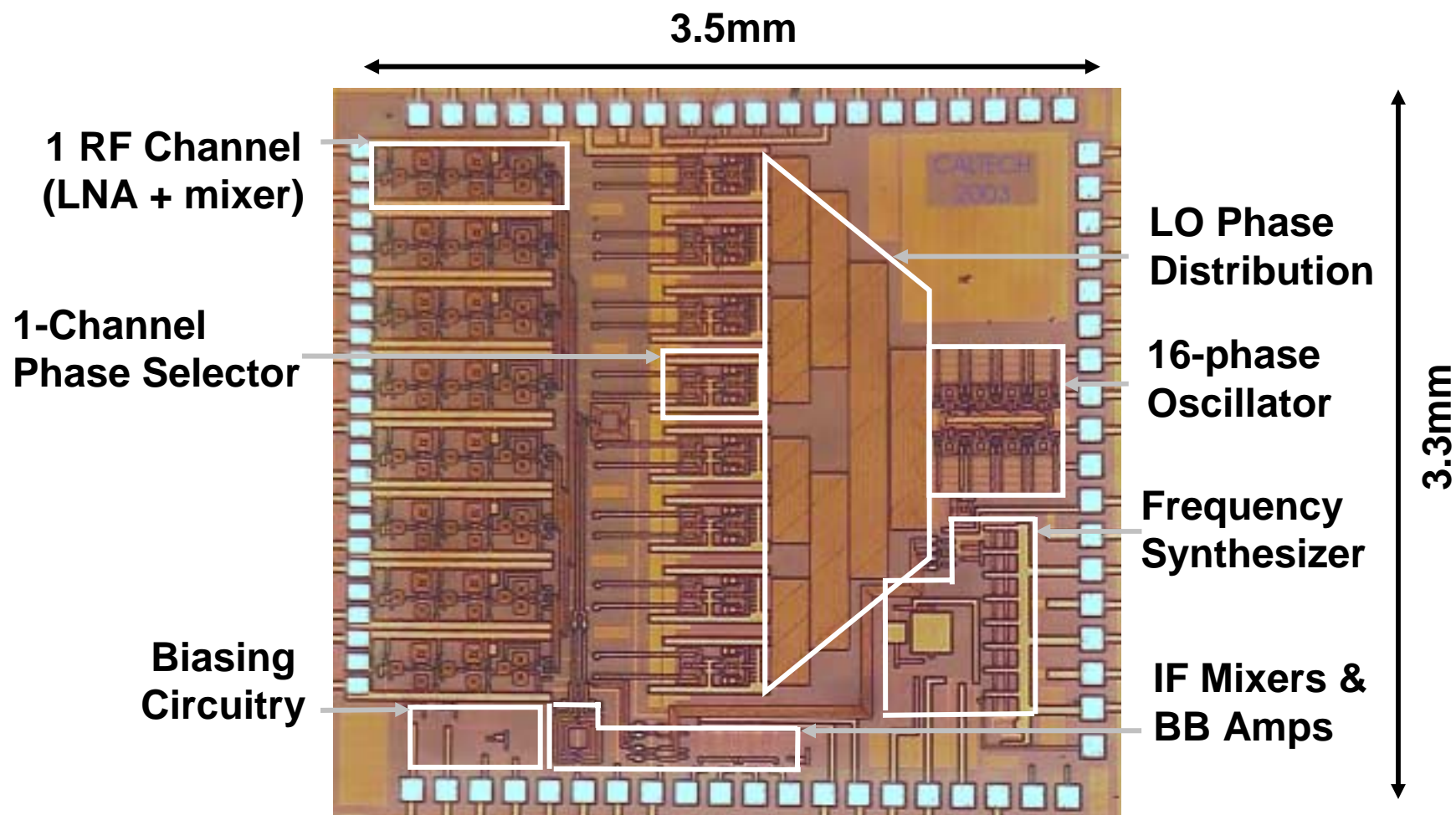
- The adopted distribution tree and phasing sequence minimizes the unwanted electromagnetic coupling between paths.*

* X. Guan, H. Hashemi, A. Komijani, and A. Hajimiri, "Multiple Phase Generation and Distribution for a Fully Integrated 24-GHz Phased-Array Receiver in Silicon," *to be presented at RFIC'04*, June 2004.

Outline

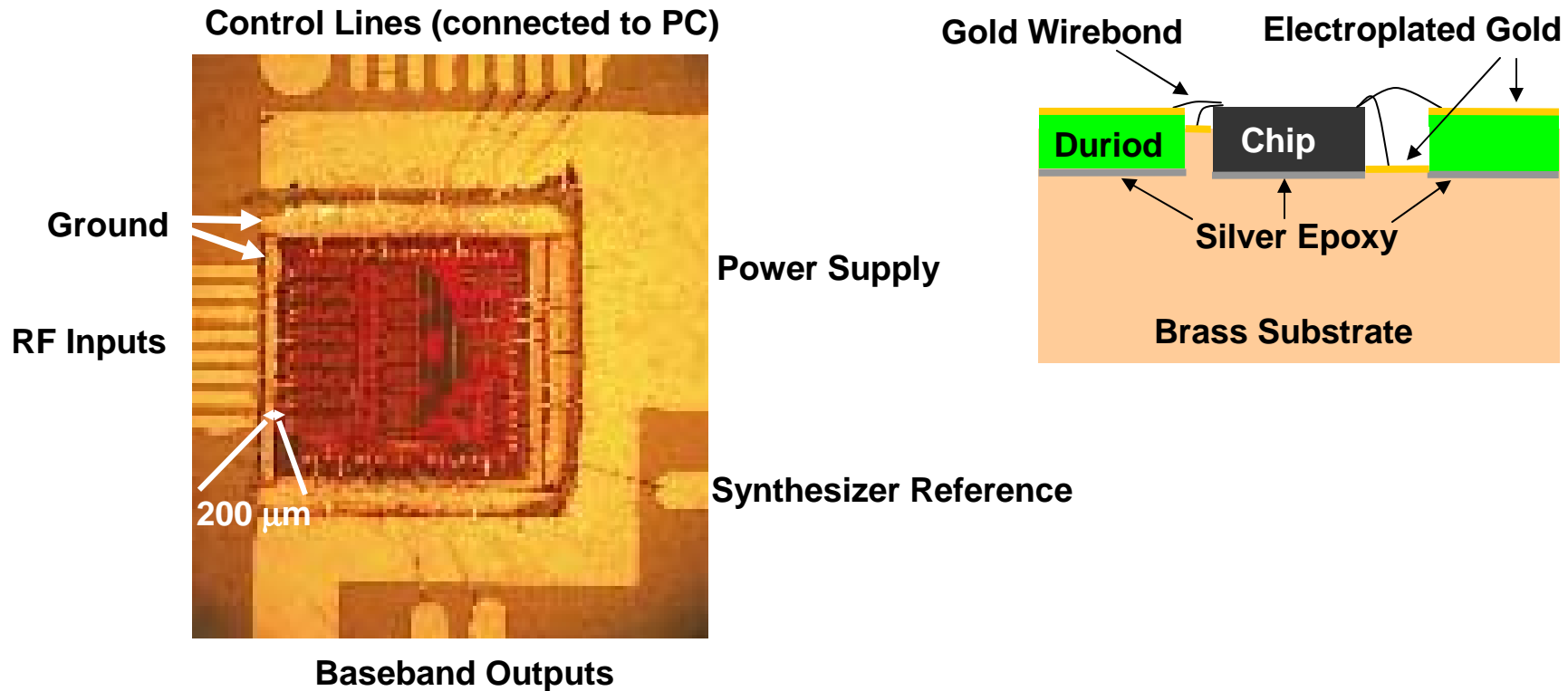
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Die Microphotograph



Implemented in a SiGe Process ($f_{T,HBT}=120\text{GHz}$, $L_{CMOS}=0.18\mu\text{m}$)

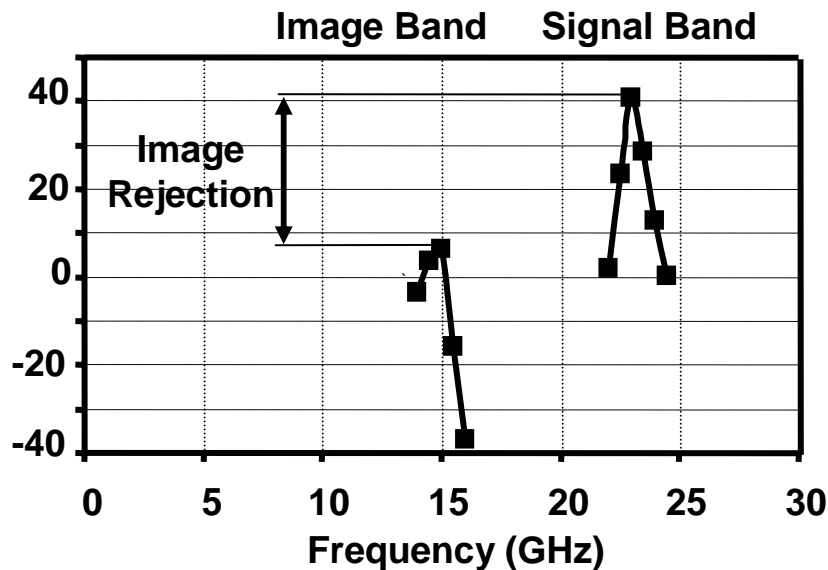
High Frequency Test Setup



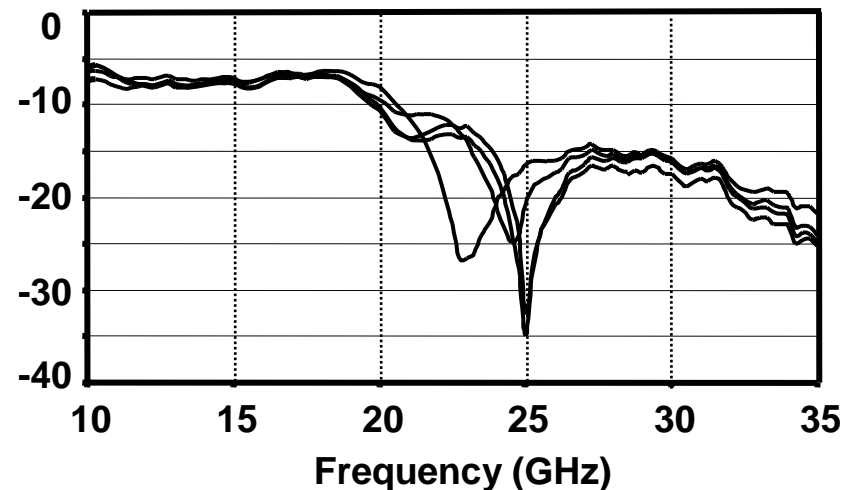
- Short and symmetric connections to multiple inputs,
- Efficient grounding at high frequencies,
- Compatible with patch antenna technology.

Small Signal Response

Single Path Gain [dB]



Input Reflection, S_{11} [dB]

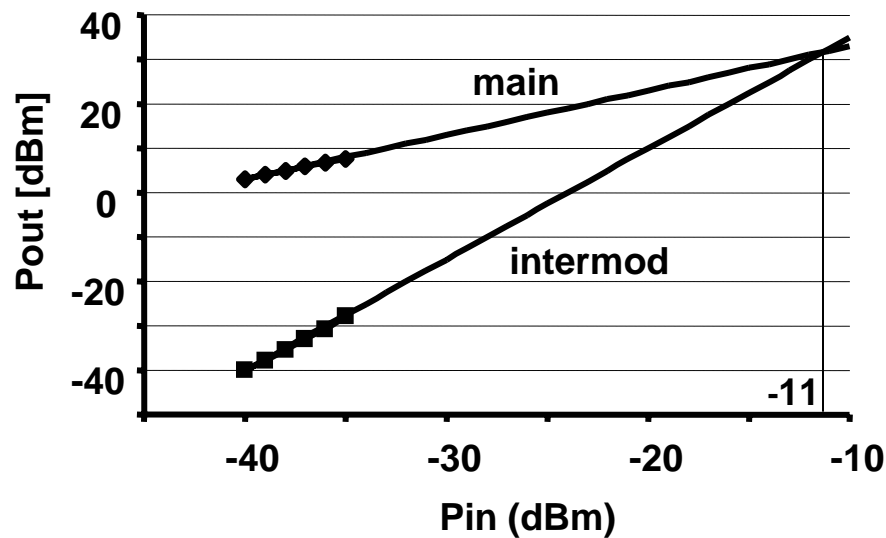


- 18dB larger signal gain for the 8-path array,
- 9dB SNR improvement in the 8-path array,
- Image rejection can be further enhanced by using narrowband antennas¹.

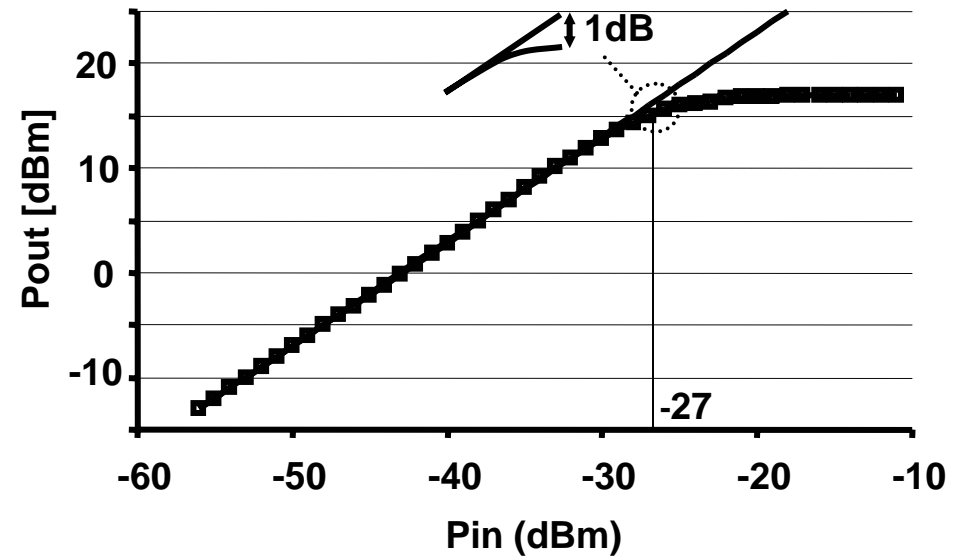
* D. Lu, M. Kovacevic, J. Hacker, and D. Rutledge, "A 24-GHz Active Patch Array," *International Journal of Infrared and Millimeter Waves*, pp. 693-704, May 2002.

Single Path Large Signal Behavior

Two Tone Test *



Compression Point

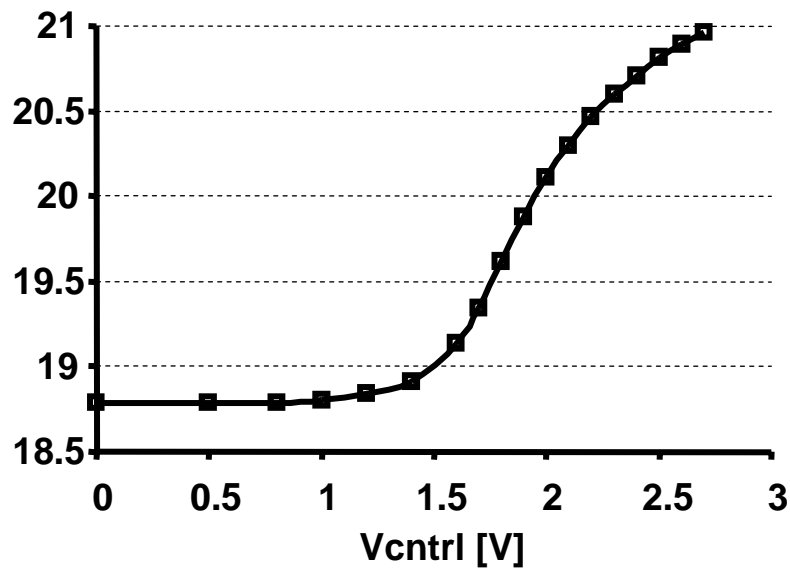


- Intermodulation slope is 2.5dB/dB,
- Higher-order nonlinearity affect the system.

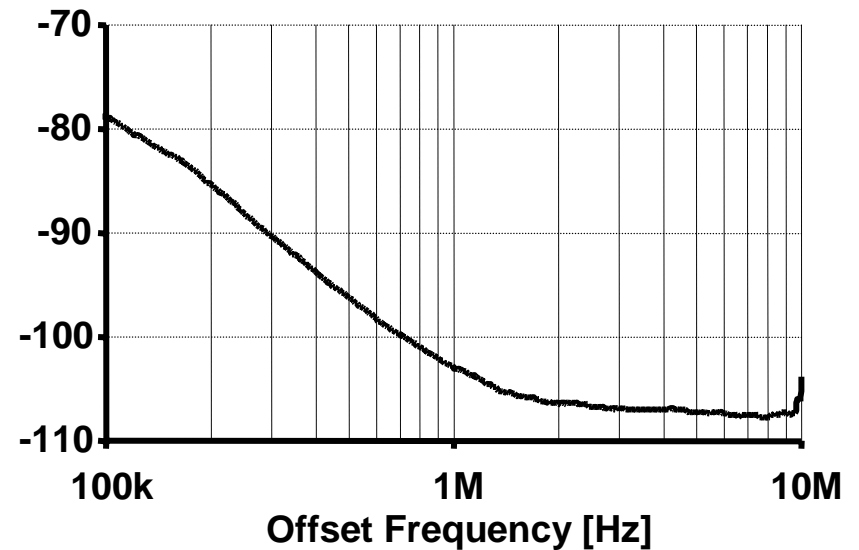
* Two in-band tones with 5-MHz separation are applied.

16-Phase Voltage-Controlled Oscillator

VCO Frequency (GHz)



Phase Noise (dBc/Hz) *

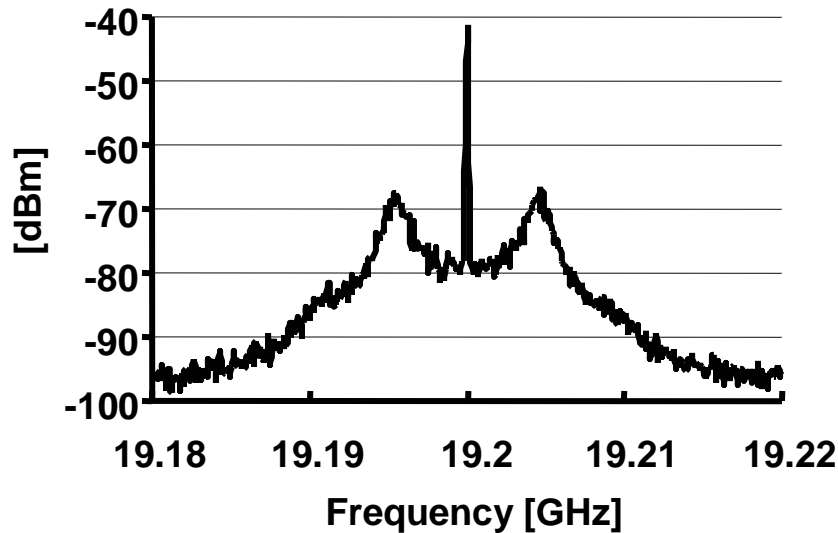


- Non-intrusive measurement using a pick-up coil,
- Phase noise variations with frequency in stand-alone VCO.

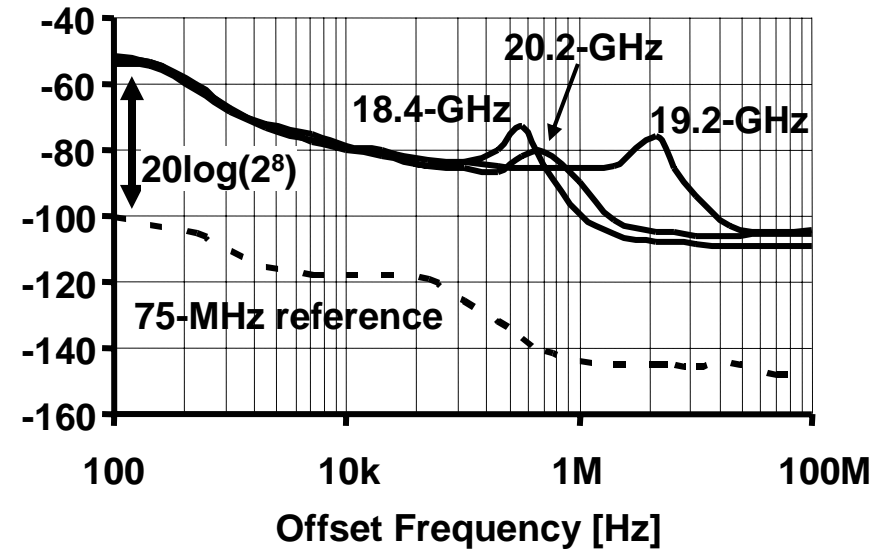
* Phase noise curve for VCO frequency of 18.7-GHz.

19-GHz Frequency Synthesizer

Locked Spectrum



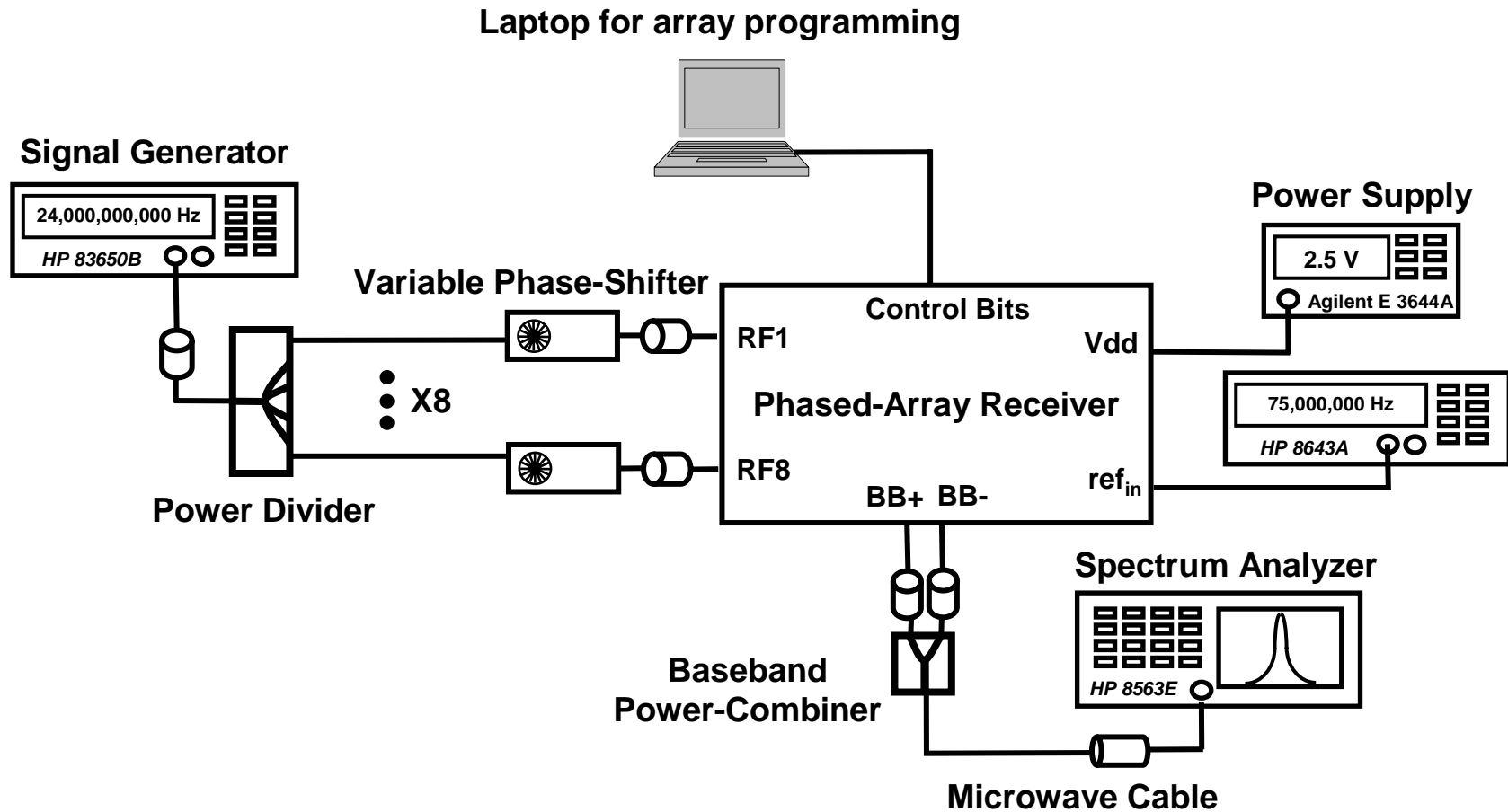
Phase Noise (dBc/Hz)



- Synthesizer locking range is greater than 2-GHz, *
- Similar in-band phase noise for all locked frequencies,
- Phase noise measurements limited by reference noise.

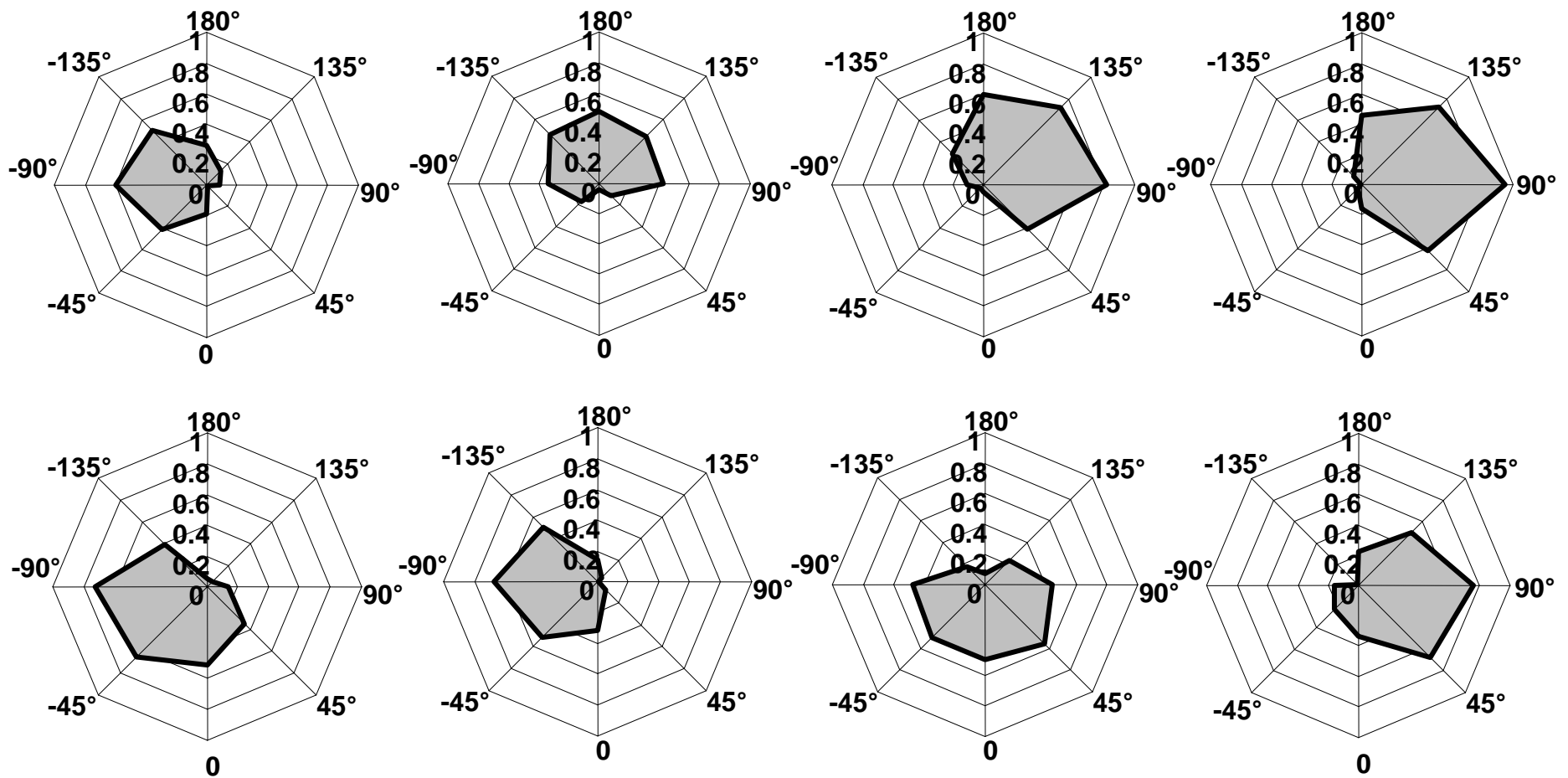
* By varying the reference frequency

Array Measurement Set-up

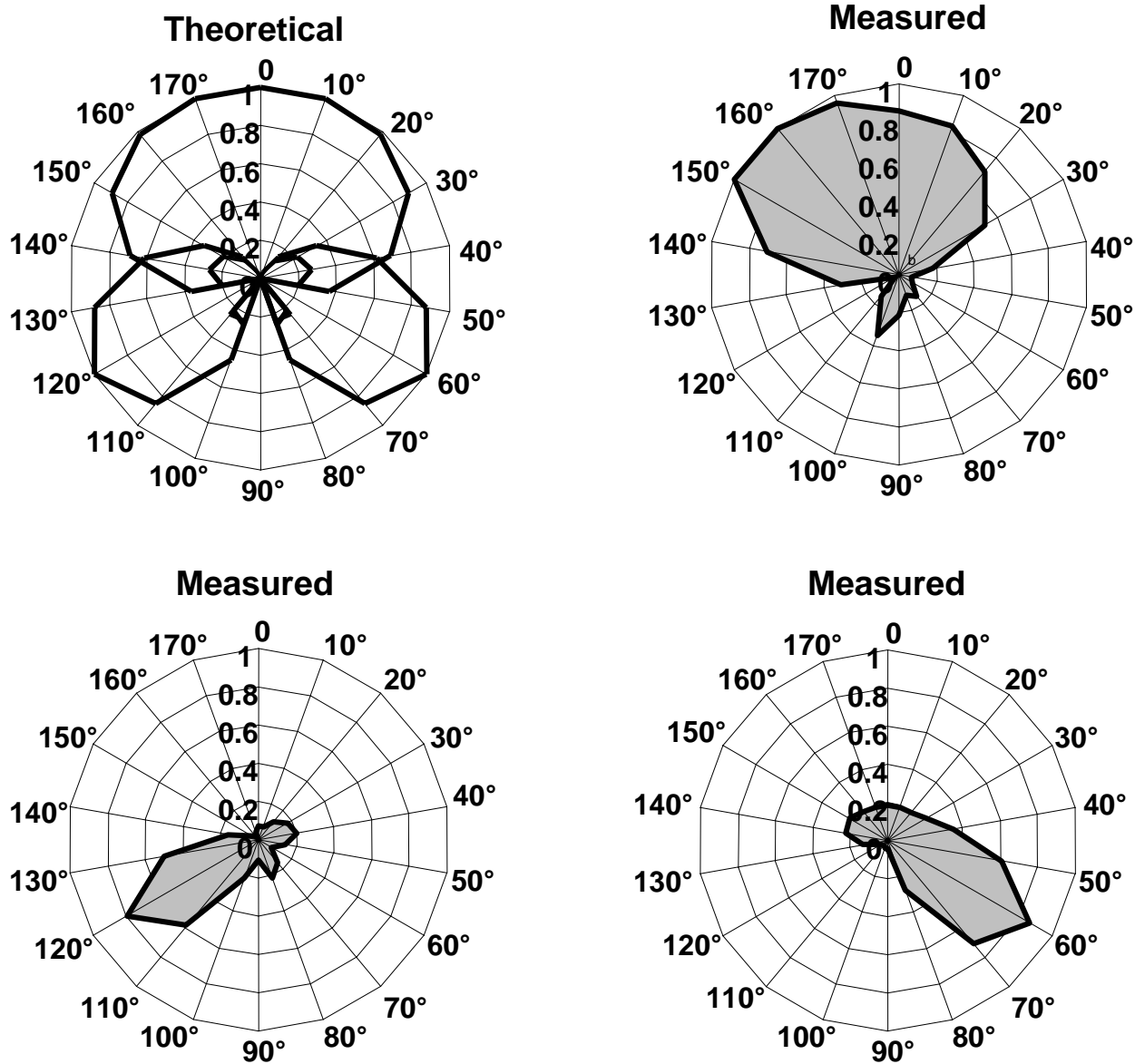


- Phase-Shifters at input emulate propagation delay.

2-Path Array Patterns



4-Path Array Patterns



Measured Performance Summary

<i>Signal Path Performance (per path)</i>	
Peak Gain	43dB
Noise-Figure	8.0dB
Input-Referred 1dB Compression Point	-27dBm
Input-Referred Intercept Point	-11.5dBm (2 tones 5MHz apart)
On-chip Image Rejection	35dB
Input reflection Coefficient (S_{11})	-10 to -20dB
<i>LO Path Performance</i>	
Synthesizer Locking Range	2 GHz (10%)
K_{VCO}	2.1 GHz/V @ 19.2GHz
VCO Phase-Noise	-103dBc/Hz @ 1MHz offset from 18.7GHz
<i>Complete Receiver Performance (8 paths)</i>	
Total Array Gain	61dB
SNR Improvement	9dB
Beam-steering Resolution (forward looking)	<10°
Beam-forming Peak-to-Null Ratio	up to 20dB (measured for 4 path)
Power Dissipation @ 2.5V	364mA 287mA (w/o biasing and baseband buffers)
<i>Implementation</i>	
Technology	SiGe, 120GHz HBT, 0.18 μ m CMOS
Die Area	3.5mm x 3.3mm

Summary

- Multiple antenna offer more efficient solutions at higher frequencies.
- 24-GHz is a good candidate for a variety of future wireless communication schemes and automotive radar applications.
- Phase shifting has been performed at the local oscillator path using a multi-phase synthesizer and symmetric distribution networks.
- The first fully-integrated phased-array system at 24-GHz using a silicon technology has been demonstrated.

Acknowledgements

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- R. Aparicio, R. Chunara, A. Komijani, A. Natarajan, D. Lu, N. Wadefalk, A. Shen, and Prof. D. Rutledge from Caltech.